DESIGN OF EIZAKKAR COMPARATOR FOR HIGH SPEED AND LOW POWER CONSUMPTION USING CMOS TECHNOLOGY

B. Saritha
Department of ECE
Vaagdevi College of Engineering
Telangana, India.
balabadrasaritha@gmail.com

Dr.B. Satheesh
Assistant professor
Vaagdevi College of Engineering
Telangana, India.
srisabharath27@gmail.com

***Abstract* - The aim of this Research proposal is to design and build dynamic comparator that outperforms the conventional Strong-Arm latch (single tail comparator and double-tail latched comparator) in terms of delay and power efficiency. A comparator plays an important role in designing the desired high-resolution, high-speed and low power analog-to-digital data converter. Among different architectures, CMOS dynamic latched comparators find wide usage in Analog-to-Digital Converters (ADCs) thanks to their high-speed, low power consumption and ability to produce rail-to-rail outputs. The Strong-Arm latch is one of the most common dynamic comparators used in ADC designs. In this Research proposal, an EI-zakker comparator for high speed and low-power dynamic comparator topology is proposed and compared to the conventional Strong ARM latch type of single tail and double tail latch in terms of delay, power consumption and speed. Simulation results show that the proposed architectures consume 40% to 50% less power than the Strong-Arm latch for the same input referred voltage of 1.8v. Additionally, the speed of proposed EI-Zakker comparator design is insensitive to input common-mode variation and outperforms the Strong-Arm latch type for low Vcm (common mode voltage) values. The Strong-Arm latch types and proposed EI-Zakker comparator architecture are simulated on the same technology using 180nm TSMC CMOS Technology. The measurement results confirmed the better performance of the proposed designs by showing 46% less power consumption than the Strong-Arm latch type of single tail and double tail comparators with similar input-referred voltage. The proposed EI-Zakker topology offers a low-power, wide common-mode input range solution for high-precision comparator design.**

Keywords— Comparator, Strong ARM comparator, CMOS, EI-Zakker comparator, double tail latch type comparator, low power.

I. INTRODUCTION

Analog-to-Digital converters (ADCs) are continuously being pushed to their performance limits and have seen tremendous decrease in their power consumption over the last few years. In high-speed analog to digital conversions (ADC) comparators play a major role during the operation an operation amplifier is one of the most commonly used devices in electronic circuits. An operational amplifier with open loop configuration is called as a comparator. Dynamic comparators are the essential building block in many mixed signal conditioning circuits. The widespread use battery powered applications demand low power signal processing circuits, resulting in the wide spread use of dynamic comparators. Strong latch type dynamic comparators and its variants are widely used owing to their negligible static power consumption.

1.1 BASICS OF CMOS COMPARATOR

Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter.

The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator are shown in fig.1.1, this comparator can be thought of as a decision-making circuit.

1.2 Definition

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison.

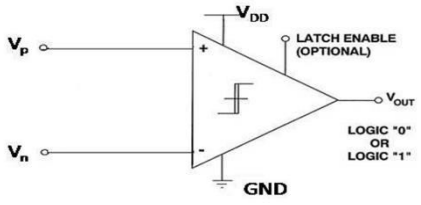

Figure 1: Schematic of Comparator

Now if Vp, the input of the comparator is at a greater potential than the Vn, the reference voltage, then the output of the comparator is logic 1, where as if the Vp is at

a potential less than the Vn, the output of the comparator is at logic 0.

If Vp > Vn, then Vo= logic 1.

If Vp < Vn, then Vo= logic 0.

II. LITERATURE SURVEY

Comparators are the core of an analogue-to-digital converter (ADC), The Dynamic Comparator performance requirements, including noise, offset, speed, and energy consumption, are becoming higher and higher. Many comparators are designed to meet these requirements, but their design approaches are different.

From analysis and design of analog integrated circuit by Razavi [8]. The single tail comparator as show in fig.1 is the first in class of dynamic comparator and widely used as regenerative comparator [7]. It has many applications, such as A/D converters and wire line receivers in virtue of its fast decisions and high-power efficiency due to the strong positive feedback and non-existence of static power consumption. The circuit only functions as a comparator when the input clock value is one. However, because of the single stage [7], there are many problems such as large voltage headroom and considerable kick-back noise [7, 4].

To overcome the limitations of single tail by reducing the stacking effect, delay and increasing the speed. The double –tail dynamic latched comparator proposed by D. Schinkel et.al can be seen in fig 2.

By separating the pre-amplifier stage from the regenerative latch stage in H.S Bindra, C.E Lokin [5]. The double-tail latch-type architecture (Fig.2). This design has less stacking of transistors and therefore can be used at low supply voltages, which is the advantage of this topology. And to mitigate the problems by separating the pre-amplifier stage from the latch. A small tail current for the pre-amplifier (for higher gm/ (ID1, 2) and lower noise) and a large tail current for the latch (for faster regeneration) should be set [2].

single-tail comparators offer fast response times but suffer from high power dissipation and kickback noise, whereas double-tail comparators are designed to address these limitations by providing lower power consumption, faster activation, and reduced kickback noise, making them suitable for high-speed, low-voltage, and power-sensitive applications like modern Analog-to-Digital Converters (ADCs). Samanesh Babayan and Reza Lotfi note that adding a few transistors to a double-tail design can further reduce power and delay.

V.S. Bagad, Y. Uma Devi, and Naveen Rathee acknowledge the single-tail comparator's high input impedance and robustness against noise and mismatch. They also note the disadvantage of high-power supply consumption due to transistor stacking, which also increases delay.

Venkata Sai Rohit Bhagaatula and Sri Harsha Gubbala emphasize the high input impedance and low static power consumption that result from the single-tail architecture. However, they highlight the challenge of operating at low voltages due to the stacked transistors.

Samanesh Babayan-Mashhad and Reza Lotfi are key proponents of the double-tail design, focusing on its superiority in low-voltage and low-power applications. In a 2014 IEEE publication, they analyze and propose a modified version of the conventional double-tail comparator that further reduces delay and power by adding a few transistors.

Rahul Priyadarshi, Rahul Nagore, Pramod Kumar Jain, and R. S. Gamed analyze the double-tail structure as a solution for low-power and high-speed applications. They confirm its ability to operate at low supply voltages due to less transistor stacking compared to the single-tail design.

The same holds true for another comparator: the EIzakker comparator [4], which is shown in Fig.4.. In this research paper we present a detailed analysis of the latch- type dynamic EIzakker comparator. Also, the design methodology and operational details. The EIzakker comparator has cross coupled latched region is compared with the clocked tail transistor M8 in (Fig.4). Section III revisits the single tail comparator [4] and its variants double tail Latch type comparator [6]. Section IV describes the operation of the proposed dynamic EI-zakker comparator and Simulation Results. Based on the circuit of Fig.4, we show the power consumption and delay. Section V presents the Results and Discussion of both the compactor with proposed comparator. Section VI Conclusion and feature scope.

III. EXISTING SYSTEM DESIGN

1. Single Tail comparator Working Operation:

The Single Tail comparator circuit shown in Fig.2. The circuit's name comes from its single "tail" transistor, which is connected to the ground and controls the circuit's operation with a clock signal. In this the tail transistor present to control the circuit functioning. The clock is provided to improve the functionality of the circuit as it controls the transistors switching them ON and OFF. The comparator circuit works in two phases namely Reset phase and Comparison phase.

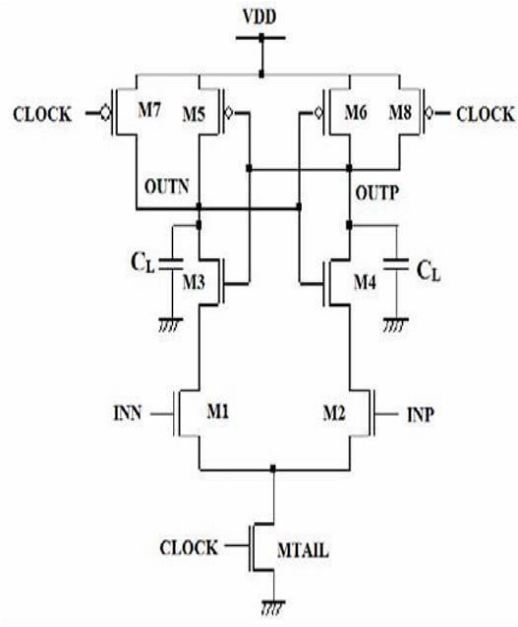

Fig.2 Single tail comparator (Schematic diagram of conventional dynamic comparator)

Reset phase:
When clock=0 is given to the transistors. The M tail transistor gets OFF and the transistors M7, M8 are ON. The nodes outn and outp are charged to VDD and logic 1occurs at both the nodes. This is called Reset phase. Here the output values do not depend on the INN and INP values.

Comparison phase: occurs only when clock =1The transistors M (3, 4, 5, 6) work as a regenerative latch which provides feedback to the circuit. The outn node acts as input to M6, M4 transistors and outp node acts as input to M5, M3. Now clock=1 is given to the transistors. M tail gets ON and corresponding M7 and M8 gets off. Both the output nodes outp and outn which had been pre-charged to VDD. Start to discharge with different discharging rates depending on the corresponding input voltages (INN and INP). Hence M5 gets ON those results in latch generation of the inverters M3, M5; M4, M6. Since INN>INP that implies VINN>VINP and M1 gets ON, M2 gets OFF resulting in grounding of the voltage at outn and maximum voltage at outp (outn<outp). The revere occurs when INN<INP i.e., outn>outp. This is called comparison phase of the circuit.

The stacked structure of the strong arm requires large voltage headroom which becomes problematic in low voltage deep submicron CMOS technology. If we want to increase the drive current of the latch for faster operation, we will have to increase the size of the tail transistor M Tail. Therefore, the strong arm has only one tail transistor. Increase the size of tail transistor will yield to an increase in the drain current of M1-M2 during amplification consequently; transistors M1 and M2 operate in saturation region in shorter time. As capacitance at nodes A and B discharge faster, voltage mismatch from M7 and M8. The regenerative latch is not isolated from the input stage.

2. Double Tail Latch type comparator Working Operation:

This architecture over comes the disadvantages of the Strong-Arm latch (large voltage headroom, kickback noise) by separating the per-amplifier stage from the regenerative latch stage [5]. This two-stage architecture with differential NMOS input pair can provide near-VDD operation, the common mode current of the pre-amplifier and the regeneration speed of the latch can be controlled independently.

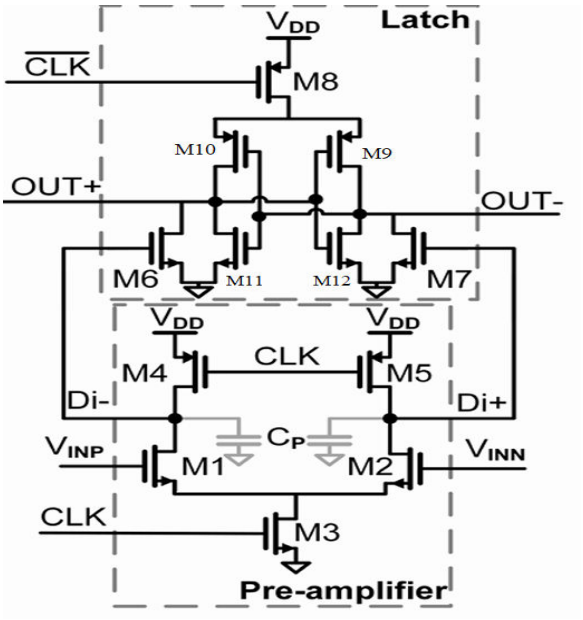

Fig.3 Schematic of Double –Tail Dynamic Latched Comparator

A Small tail current for the pre-amplifier (for higher gm / (ID, 2) and lower noise) and a large tail current for the latch (for faster regeneration) should be set.[2].

The operation off the conventional double tail comparator is as follows:
i. During the reset phase, clock =0, Di nodes are pre-charged to VDD through PMOS switches M4-M5. As Di nodes control the gates of NMOS transistors M6-M7, the output nodes of the latch stage get reset to ground through M6-M7. Both tail transistors, M3 and M8 are OFF during the reset phase.

ii. During evaluation phase, clock=1, Tail transistor M4 of the pre-amplifier stage turns ON and current flows through the drain nodes of the input pair M1-M2. Di nodes start to discharge from VDD at different rates proportional to input voltages. Therefore, a certain gain builds up from input to Di as the voltage difference Di+ - Di- becomes greater than VINP – VINN. The output Di of preamplifier is connected to the output nodes of the regenerative latch through M6-M7. Regeneration at the latch stage start when Di+ and Di-

discharge down to the point where M6-M7 cannot ground the output nodes anymore. At this point, the tail transistor of the latch M8 is ON and the cross-coupled inverters in the latch stage start to regenerate the small voltage difference between the output nodes OUT+, OUT- and one output is eventually brought up to VDD while the others fall to ground.

Clk and clkb requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from input stage at very limited time. Now if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M8 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M8 to M6/M7 through M9/M10 [5].

3.1 Results of existing system design:

1.Schematic circuit diagram of the Single tail comparator implemented 180nm technology in TSMC library for Single tail comparator design. The Schematic track diagram of the Single tail comparator is given below Figuer.1 (a). Structure: It uses a single tail current source (one transistor) to bias both the input differential pair and the latch stage.

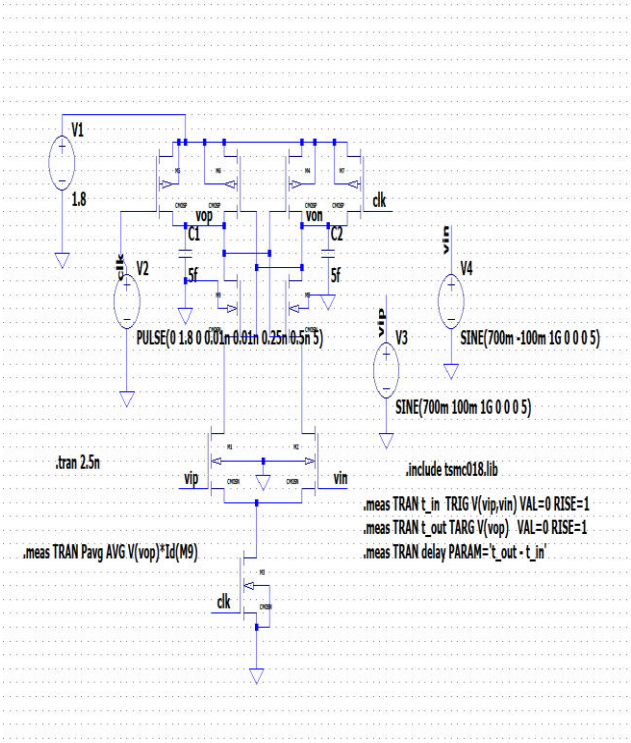

Fig2.1 Schematic circuit diagram of the Single tail comparator

Simulation Result:

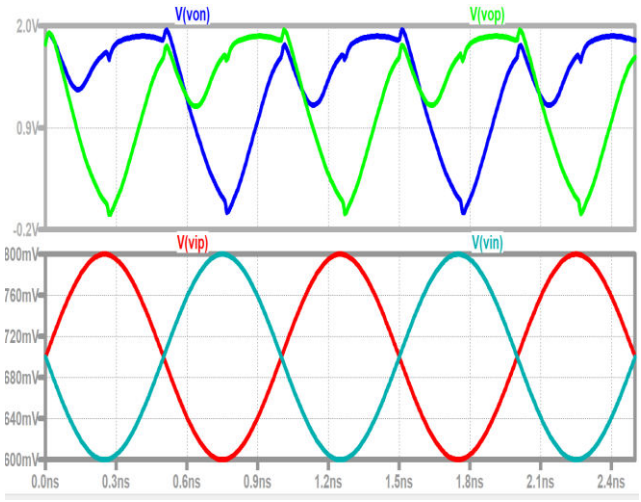

Fig 2.2 Transient response of single tail comparator

(VDD=1.8V, fCLK=1GHz, VIN=700mV)

2. The Schematic track diagram of the Double tail latched comparator implemented 180nm technology in TSMC library is given below Fig.3.1. Structure: It utilizes two separate tail current sources. One tail current bias the input differential pair, while the other tail current biases the latch stage.

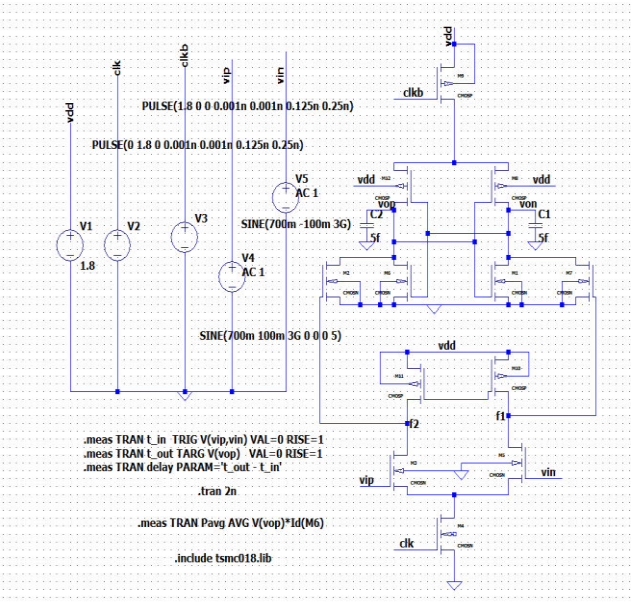

Figure 3.1 schematic diagram of double tail latched comparator

In double tail latched comparator, we are using two tail transistors have down side tail has less width compare to upper tail. This two-stage architecture with differential NMOS input pair can provide near-VDD operation thanks to the greater input common-mode range [5]. Moreover, thanks to the separate tail transistors for pre-amplifier and latch stages, the common mode current of the pre-amplifier and the regeneration speed of the latch can be controlled independently

Simulation results:

The comparator transient simulation results are shown in figure 3.2 With C set to 5Ff, the DC offset voltage verses the time period.

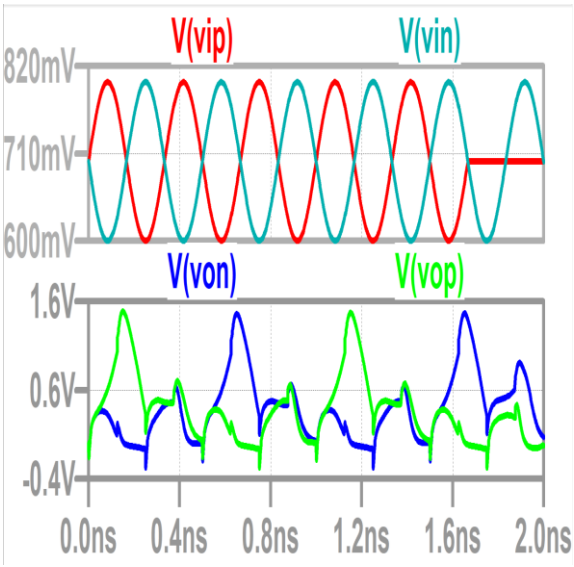

Fig. 3.2 Transient response of double tail latched comparator

(VDD=1.8V, fCLK=3GHz, VIN=700mV)

IV. PROPOSED SYSTEM DESIGN

The main innovation of the EI-zakker comparator is its approach to timing and discharging. Unlike the standard double-tail design, which separates the input and latching stages with distinct current paths, the EI-zakker design cleverly delays the activation of the regenerative latching stage until the pre-amplifier has built up a sufficient differential voltage. This minimizes the energy wasted by preventing internal nodes from discharging completely to the ground. This topology has two stages: a pre-amplifier stage, and a latch stage. Each stage will be evaluated in depth. The double tail latch type architecture [5] of Fig.3.3 suffer from poor optimization of energy consumption for a given SNR due to the fact that the pre-amplifier as well as the regenerative latch start operating at the same time. Since at the start of comparator operation, the differential voltage at the output of pre-amplifier is approximately zero, the latch stage conducts without developing any appreciable SNR. This makes it less attractive for low power application such as medium to high resolution SAR ADCs. A more optimum solution from the perspective of energy consumption is to delay the conduction of the latch stage, until the time a sufficient voltage gain is developed across the pre-amplifier output nodes.

For use in SAR ADCs, the EI-zakker comparator proposed by (van EI-zakker et al.) show in Fig.4. In it, the pre-amplifier stage is same as in [4], but in contrast to the work in [4], the output of the pre-amplifier is fed to PMOS transistor M6/M7 which is embedded in the latch stage.

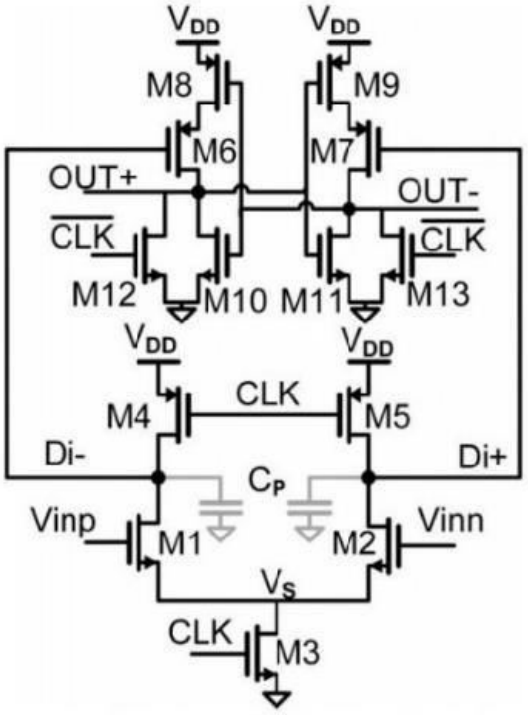

Fig 4: Proposed design

Unlike the clocked tail transistor M8 in Fig.3 there is no explicit tail transistor in the latch stage for the architecture [6] in Fig.3.The whole circuits can be divided in two parts: the pre-amplifier with a differential input (Di+, Di-) as well as a differential output (Out+, Out-) and the latch stage with a simple voltage amplifier and a positive-feedback amplifier.

4 .1 EI-zakker comparator Operation

The EI-zakker comparator operation has two phases:

When (CLK=0), transistors M4, M5, M8, M9, M11 and M13 are conducted, while transistors M3, M6, M7, M10, M12 are closed, which means the output of the pre-amplifier (D+, D-) are at VDD and the latch stage only begin to conduct when the common-mode voltage of the output is below the threshold value of M6, M7.

At the regeneration stage (CLK = VDD), At the same time, differential voltage is added to Vinp / Vinn. Thus, when Di- , D+ falls low enough. When comparison start M3 turn on. The tail transistor produces the tail current helps improve isolation between the stages. Which means M6 and M7 become conducted, the sufficient differential voltage (gain) at its input to perform the regeneration operation, by connecting M6/M7 to the latch stage that we called it as intermediate control circuit, it allows the faster decision making and less power consumption. Latch stage is also called positive feedback circuit.

In double tail comparator and EI-zakker comparator Tail transistor working is same; the only difference is adding M6/M7 transistors to the latch stage. By using control transistor M6/M7 in latch stage the output capacitor is not fully discharged to ground. Because of this it will take less time to take the decisions.

4.2 Results of proposed system design:

Figure 4 shows the EI-zakker comparator (energy efficient two-stage comparator). The circuit is almost same as Figure.3 except the output latch stage. By modifying the output latch stage during reset phase (clk=0V and clkb=VDD), the drain diffusion capacitances of PMOS transistors M1 and M2 & NMOS transistors M11 and M12 is much lesser than the Ni node capacitances. And hence it can be operated in lesser power dissipation and higher speed than the previous comparator. But still the clocking problem was not solved since clk and clkb is operating in same clock signal as that was in previous comparator.

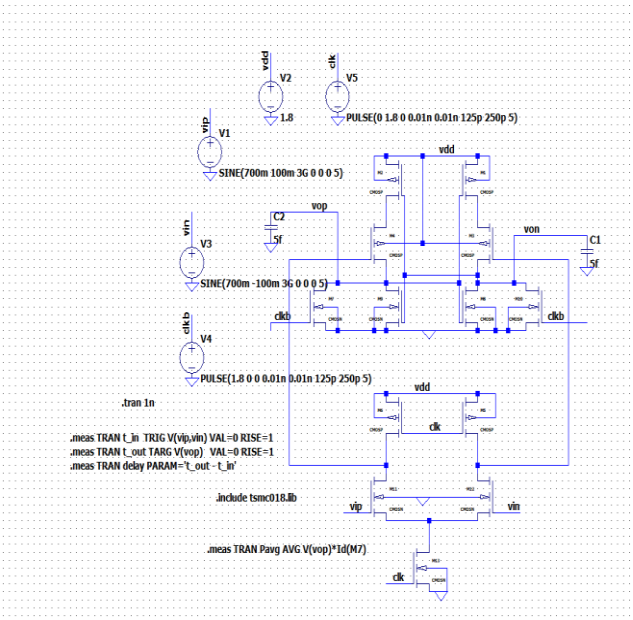

Figure 4.1 Schematic circuit diagram of the EI-Zakker dynamic comparator

The pre-amplifier in [3] is the same simple NMOS dynamic amplifier as in standard double-tail comparator [2]. The output of the pre-amplifier is connected to a pair of PMOS transistors implanted in the output latch. Upon the beginning of the comparing operation, Vip and Vin are at VDD and M3, M4 are off. The output latch starts after pre-amplifier output voltages drop below the threshold voltage of M3, M4, which compared to the standard one, is a major energy efficiency improvement. By modifying the output latch stage during reset phase (clk=0V and clkb=VDD), the drain diffusion capacitances of PMOS transistors M2 and M1 & NMOS transistors M5 and M6 is much lesser than the Ni node capacitances. And hence it can be operated in lesser power dissipation and higher speed than the previous comparator.

Simulation results:

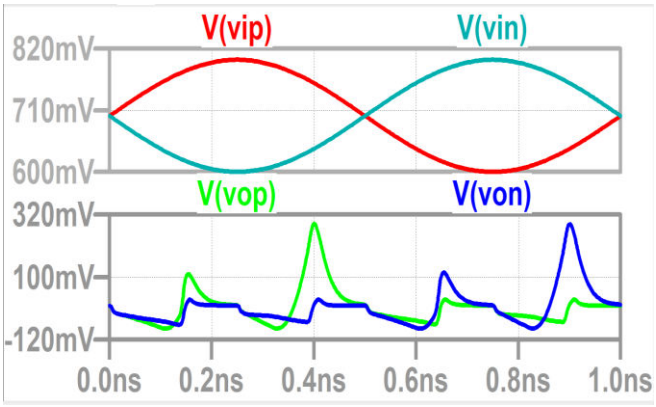

Fig.4.2 transient response of EI-zakker comparator (VDD=1.8V, fCLK=3GHz, VIN=700mV)

A power and delay of an EI-Zakker comparator design in the manometer scheme. For comparison, this paper employed the EI-Zakker dynamic comparator design. This paper implemented 180nm technology in TSMC library for EI-Zakker dynamic comparator design. The Schematic track diagram of the EI-Zakker dynamic comparator is given below Figuer.4.1

To perform power calculation for a dynamic comparator A transient simulation in LTSpice predicts how a circuit's voltages and currents change over time after a stimulus.

Average Power calculation

in SPICE using the. trans directive, simulate the circuit and use the ". measure Pavg" command to find the average power, which is calculated as the average current times the supply voltage across the simulation period.

Delay Calculation

The delay is then determined by measuring the time it takes for the output to cross a certain threshold after a specific input differential voltage is applied. You should also measure the output voltage against the input voltage with the. trans directive.

V. RESULTS AND DISCUSSION

A new dynamic comparator using positive feedback which shows better noise response, higher speed, lower power dissipation than the conventional dynamic latched comparators has been proposed & targeted for ADC application. To compare the performance of the proposed comparators with previous works, each circuit was simulated in LTSpice analog design environment. Technology used is TSMC 180nm technology with VDD=1.8V as supply voltage. In the proposed design, the back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. The

proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature.

Table.1

Reduced performance of total dynamic power and delay for existing and EI-Zakker comparator design

Comparator	Single tail comparator	Double tail latched comparator	EI-Zakker comparator
CMOS Technology	TSMC 180nm	TSMC 180nm	TSMC 180nm
Supply Voltage	1.8v	1.8v	1.8v
Clock Frequency	1GHZ	3GHZ	3GHZ
Propagation Delay	2.21ns	1.94ns	0.87ns
Dynamic power	30uw	1.23uw	0.567uw

VI. CONCLUSION AND FUTURE SCOPE

To compare the performance of the proposed comparators with previous works, each circuit was simulated in LTSpice analog design environment. Technology used is TSMC 180nm technology with VDD=1.8V as supply voltage. Table 1 shows the result summary. From Table 1 we can say that the dynamic power dissipation of proposed comparator is 46% less than the double tail latched comparator. 45% less delay compare to double tail latched comparator. And hence it can be operated in lesser power dissipation and higher speed than the previous comparator. But still the clocking problem was not solved since clk and clkb is operating in same clock signal as that was in previous comparator.

This proposed design Implementation in advanced nodes (e.g., 65nm, 28nm) also. Integration in full ADC design and Layout & post-layout simulations. For Noise reduction use noise optimization techniques, ASIC implementation for real-time systems.

REFERENCES

[1] B. Goll and H. Zimmermann, A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65, “IEEE Trans. Circuits Syst. II, Exp. Brief, vol. 56, no 11, pp. 810-814, Nov. 2009.

[2] H. Jeon, “Low-power high-speed low-offset fully dynamic CMOS latched comparator,” Master’s thesis, Northeastern University, Boston, Massachusetts, 2010.

[3] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, “Yield and speed Optimization of a latch-type voltage séance amplifier.” IEEE J. Solid State circuits, vol. 39, no.7, pp. 1148-1158, Jul. 2004

[4] D. Schinkel et. al, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup Hold Time", 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, 2007, pp. 314 605.

[5] H. S. Bindra, C. E. Lokin, D. Schinkel, A. J. Annema, and B. Nauta, “A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise,” IEEE Journal of Solid-State Circuits, vol.53, no.7, pp.1902–1912, July2018.

[6] M. van EIzakker et.al, "A 10-bit Charge-Redistribution ADC Consuming 1.9µW at 1MS/s", in IEEE Journal of Solid-State Circuits, vol. 45, no. 5, pp. 1007-1015, May 2010.

[7] TSMC 180nm Process Design Kit Documentation.

[8] R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation.

[9] B. Goll and H. Zimmermann, A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65, “IEEE Trans. Circuits Syst. II, Exp. Brief, vol. 56, no 11, pp. 810-814, Nov. 2009.

[10] Heung Jun Jeon and Yong-Bin Kim, “A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator”, IEEE, 2010.

[11] Razavi Behzad, “Design of Analog CMOS Integrated Circuits”, New York, NY: McGraw-Hill, Inc., 2000.

[12] Sansen Willy M.C., Analog Design Essentials”, Neatherlands, Springer International Edition, 2006.

[13] Dutta Ramen, “CMOS Voltage Comparator”, Advanced VLSI Design Lab, IIT Kharagpur. [Online]. Available: conf05.iitkgp.ac.in/avlsi/logf/summer course/2008/c omparator.pdf [Accessed: 14 March, 2011].

[14] Allen Phillip E., Short Course Notes on CMOS Analog IC Design. [Online]. Available: http://www.aicdesign.org/scnotes10.html [Accessed: February 12, 2011].

[15] Allen Phillip E., “Lecture-360- Characterization of Comparator”. [Online]. Available: users.ece.gatech.edu/pallen/.../L360-Char_Comparators-2UP.pdf [Accessed 20 February, 2011].